# SCALABLE PACKET BUFFER DESCRIPTOR MANAGEMENT IN ATM TO ETHERNET BRIDGE GATEWAY

## ABSTRACT OF THE DISCLOSURE

Systems and methods for scalable packet buffer descriptor management in ATM-Ethernet bridge gateways are disclosed. An ATM-Ethernet processor interfacing between an ATM processor and an Ethernet network processor generally includes a packet buffer pointer ring containing ATM processor packet buffer pointers for managing traffic from the Ethernet network processor to the ATM processor, and a packet descriptor ring and a data buffer for managing traffic from the ATM processor to the Ethernet network processor. The packet descriptor ring contains packet descriptors each including an ATM-Ethernet packet buffer memory address in the data buffer. The ATM processor may be in communication with a SONET framer while the Ethernet network processor may be in communication with an Ethernet MAC.